

of record, whether considered alone, or in combination, fail to either teach or suggest Applicants presently claimed invention.

More specifically, Applicants claimed invention is directed to improved semiconductor structures and manufacturing techniques that significantly increase device yields and dramatically decrease manufacturing costs. As described in the specification, a pseudo-wafer is formed by placing non-defective chip members on a substrate. The chip members advantageously are surrounded by resin except for a side on which connections are formed. This pseudo-wafer advantageously allows wafer processing to be performed among other advantages while improving yield and decreasing costs. The prior art fails to provide any teaching or suggestion whatsoever regarding this advance in the art.

Applicants note that the *Corisis* reference, United States Patent No. 5,956,236 is merely directed to an integrated circuit package support system which is purportedly designed to prevent mechanical failure of the packages at the connections to a printed circuit board. The Examiner specifically relies upon Figure 5 for the assertion that surfaces other than the surface on which the electrodes are formed are continuously covered with a protective material 14b. However, it is clear from the drawing that the top portions of each package 12 is not covered by the protective material and furthermore, only portions of the sidewalls are secured with the protective material. The *Corisis* reference fails to provide any teaching whatsoever regarding the presently claimed structure. Indeed, *Corisis* actually teaches away from Applicants unique and advantageous structure.

Accordingly, for the foregoing reasons, because the prior art of record fails to teach or suggest the claimed invention, Applicants respectfully request that the Examiner now allow all claims in the application.

Respectfully submitted,

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